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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,658	02/09/2004	Yoichi Tamaki	XA-10036	7635

181 7590 08/18/2005

MILES & STOCKBRIDGE PC
1751 PINNACLE DRIVE
SUITE 500
MCLEAN, VA 22102-3833

EXAMINER	
PHAM, LONG	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,658	TAMAKI ET AL.	
	Examiner	Art Unit	
	Long Pham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-18* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/0904*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 7-9, and 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashi et al. (Japan 2002-057219) in combination with Morishita et al. (US patent 5,508,550) and Moyer (US patent 5,374,844).

With respect to claim 1, 6, 10, 11, and 12, Takashi et al. teach a semiconductor device comprising (see figs. 1-6 and the English abstract):

a) a semiconductor layer 3 that is provided over an insulation layer 2;

b) a plurality of the same kind of bipolar transitors 18,19 that are provided on the semiconductor layer; and

c) an isolation 4-1, 4-4 is provided on the main surface of the semiconductor layer to reach the insulation layer, and provided such that the isolation surrounds a group of the plurality of the same kind of bipolar transistors.

Takashi et al. fail to teach that the the bipolar transistors are connected in parallel.

Morishita et al. teach that plurality of bipolar transistors are connected in parallel to prevent clouding effect. See col. 17, lines 60-67.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Morishita et al. into the device of Takashi et al. to obtain the above advantage.

With respect to claims 2, 3, 6, and 7, Takashi et al. fail to teach each of the emitter of the plurality of bipolar transistors is connected to a resistor made of polysilicon.

Moyer teaches connecting a polysilicon resistor to the emitter of a bipolar transistor to prevent thermal runaway. See col. 1, lines 35-40.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate the above teaching of Moyer into the device of Takashi et al. to obtain the above advantage.

With respect to claims 4, 5, 9, 13, ,14, and 15,Takashi et al. fail to teach the range for the distance between the contact holes for the base and collector.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the distance between the contact holes for the base and collector through routine experimentation and optimization to obtain optimal or desired device performance because the distance between the contact holes for the base and collector is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Further with respect to claims 10, 11, and 12, Takashi et al. in combination with Morishita et al. and Moyer teach forming a plurality of bipolar transistors in a semiconductor layer located over an insulation layer, wherein the plurality of bipolar transistors are connected in parallel, forming isolation in the main surface of the semiconductor layer to reach the insulation layer, wherein the isolation surrounds the plurality of bipolar transistors but fail to repeat the above teaching to form a second plurality of bipolar transistors in a semiconductor layer located over an insulation layer, wherein the plurality of second bipolar transistors are connected in

parallel, forming second isolation in the main surface of the semiconductor layer to reach the insulation layer, wherein the second isolation surrounds the plurality of second bipolar transistors.

However, it would have been obvious to repeat the teaching of Takashi et al., Morishita et al. and Moyer to form a second set of bipolar transistors that have the benefit of preventing unwanted charge, clouding effect, and thermal runaway.

With respect to claims 16 and 17, Takashi et al. in combination with Morishita et al. and Moyer fail to teach that the optimum current of the first bipolar transistor is greater or 1.5 times or more than the second bipolar transistor.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value or range for the optimum current for the first and second bipolar transistors through routine experimentation and optimization to obtain optimal or desired device performance because they are result-effective variables and there is no evidence indicating that they are critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

With respect to claim 18, Takashi et al. in combination with Morishita et al. and Moyer fail to teach that the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal values or ranges for the relative heat radiation and operation speed of the first bipolar transistor and the second bipolar transistor through routine experimentation and optimization to obtain optimal or desired device performance because they are result-effective variables and there is no evidence indicating that they are critical or

produce any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 571-272-1714. The examiner can normally be reached on M-F, 7:30AM-3:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Long Pham
Primary Examiner
Art Unit 2814

LP